

Typ e	L #	Hit s	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS L1	1	(Mambakkam-Sreenath.in. Venkidu-Arockiyaswamy.in. Jones-Larry-Lawson.in.) and @pd>20040518	USPAT; US-PGPUB; EPO; JPO	2004/08/23 12:51			0
2	BRS L2	225	(700/231.ccls. 361/737.ccls. 710/302.ccls. 710/301.ccls. 710/64.ccls. 710/63.ccls. 710/62.ccls. 235/492.ccls. 235/435.ccls. 235/439.ccls. 235/440.ccls. 235/441.ccls.) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 12:52			0
3	BRS L3	3	((memory smart ic chip circuit) adj1 card\$1) near5 (adapter reader terminal interface) near5 (plural\$3 many several multiple) near5 (type\$1 format\$1 standard\$1) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:29			0
4	BRS L4	0	((memory smart ic chip circuit) adj1 card\$1) near5 (adapter reader terminal interface) near5 (plural\$3 many several multiple) near5 (type\$1 format\$1 standard\$1) and @pd>20040518	EPO; JPO; DERWENT; IBM_TDB	2004/08/23 13:31			0
5	BRS L5	0	(scsi (small adj computer adj system adj interface)) near5 (simple adj display adj device) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:32			0
6	BRS L6	7	(scsi (small adj computer adj system adj interface)) near5 (display screen lcd) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:32			0
7	BRS L7	1	(scsi (small adj computer adj system adj interface)) near5 (display screen lcd) near5 (command\$3 instruction\$1) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:38			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
8	BRS	L8	0	((memory smart ic chip circuit) adj1 card\$1) near5 (adapter reader terminal interface) near5 (plural\$3 many several multiple) near5 (type\$1 format\$1 standard\$1)) same parallel and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:38			0
9	BRS	L9	1	((memory smart ic chip circuit) adj1 card\$1) near5 (adapter reader terminal interface) near5 (plural\$3 many several multiple) near5 (parallel simultaneous\$2 concurrent\$2) near5 (access\$3 read\$3 writ\$3 communicat\$3) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:39			0
10	BRS	L10	4	((memory smart ic chip circuit) adj1 card\$1) near5 (plural\$3 many several multiple) near5 (parallel simultaneous\$2 concurrent\$2) near5 (access\$3 read\$3 writ\$3 communicat\$3) and @pd>20040518	USPAT; US-PGPUB	2004/08/23 13:42			0
11	BRS	L11	0	((memory smart ic chip circuit) adj1 card\$1) near5 (plural\$3 many several multiple) near5 (parallel simultaneous\$2 concurrent\$2) near5 (access\$3 read\$3 writ\$3 communicat\$3) and @pd>20040518	EPO; JPO; DERWENT; IBM_TDB	2004/08/23 13:51			0